Set   Items   Description
S1   1617589   S (MEMORY OR MEMORIES OR RAM OR (RANDOM(1W)ACCESS(1W)MEMORY) OR EEPROM? ?
OR READ(1N)WRITE OR DRAM? ? OR SDRAM? ? OR RDRAM? ? OR DIMM? ? OR SODIMM? ? OR ECC OR PRAM
OR SIMM OR DATA()STORE OR DATA()STORAGE OR STORAGE OR READ()ONLY OR CACHE()STORAGE OR
BUFFER OR HD OR HARD()DRIVE OR AREA OR LOCATION OR STORAGE OR COMPACTFLASH OR
SMARTMEDIA OR MEMORY()STICK OR SD()MEMORY OR XD()PICTURE OR CARD OR USB()KEY OR STORAGE
OR STORE OR CACHE OR EPROM? ? OR BUFFER? ? OR DISC? ? OR DISK? ?)
S2   68261   S S1(5N)(((SECOND OR 2ND OR TWO OR 2 OR MULTIPLE OR TWOFOLD OR DUAL OR PLURAL OR
PLURALITY OR MULTIPLE? OR MULTI OR PAIR??)(2N)BUFFER? ?) OR GPU OR (GRAPHIC?
?(1W)PROCESS?(1W)UNIT? ?) OR COPROCESSOR? ? OR (COPROCESSOR? ?()READABLE))
S3   332   S S2(10N)(PAGING OR MAPP???)
S4   18908   S S1(5N)((PROPER OR CORRECT OR RIGHT OR MEET DECOROUS OR DISCREET? ? OR BELONG?
FIT OR FITTING)(3N)(LOCATION? OR ADDRESS? ? OR SPACES? ? OR POSITION? ? OR REGION? ?))
S5   63627   S S1(5N)(INDICATOR? OR POINTER? ? OR INDEX? OR GAUGE OR BELLWETHER? ? OR
DETECTOR? ?)
S6   332   S S2(100N)S3
S7   4   S S6(100N)S4

?

Subject summary

7/3K/1 (Item 1 from file: 348) Links
   Fulltext available through: Order File History
EUROPEAN PATENTS
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01778480
System and method for enhancing performance of a coprocessor
System und Verfahren zum Verbessern der Leistung eines Coprozessors
Systeme et methode pour ameliorer la performance d'un coprocesseur

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	Country	Number	Kind	Date	
Patent	EP	1450258	A2	20040825	(Basic)
	EP	1450258	A2	20040825	
	EP	1450258	A3	20070606	
Application	EP	2004003544		20040217	
Priorities	US	448402	P	20030218	
	US	448399	P	20030218	
	US	448400	P	20030218	
	US	474513	P	20030529	
	US	763778		20040122	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LI; LU; MC;
NL; PT; RO; SE; SI; SK; TR;
Extended Designated States:
AL; LT; LV; MK;
International Patent Class (V7): G06F-009/48

IPC	Level	Value	Position	Status	Version	Action	Source	Office
G06F-0009/48	A	I	F	B	20060101	20040629	H	EP

Abstract Word Count: 136
NOTE: 11
NOTE: Figure number on first page: 11

Type	Pub. Date	Kind	Text
Publication:	English		
Procedural:	English		
Application:	English		

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200435	1516
SPEC A	(English)	200435	19847
Total Word Count (Document A) 21367			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 21367			

Specification: ...Paging" refers to changing the physical address of a block of memory (a page) using mapping
hardware. A paging buffer, generally speaking, is a DMA buffer that contains coprocessor instructions to... ...buffer to a
correct memory location, from which those resources can be accessed by the coprocessor when needed. If a paging
buffer is properly generated, the location of any requisite memory resources for a particular coprocessor task(i.e., a
DMA buffer) is known.
Step 15 represents notification to a preparation thread that a paging buffer has... ...to conduct further preparation
operations on a DMA buffer prior to sending it to a coprocessor for processing. For example, since memory locations
may have changed since the creation of the original DMA buffer, the scheduler may... ...buffer with the actual location of

memory resources. Finally, the scheduler may submit both the paging buffer (if it exists) and the DMA buffer to the coprocessor (and any other auxiliary hardware) to be processed.
Steps 1 through 16 as described above...
Claims: ...to store the run list.
11. The method of claim 8, further comprising specifying a coprocessor write pointer, which indicates a location in the history buffer where the coprocessor can write... ...sampling the memory resources to determine if all required memory resources are in a proper location in the coprocessor-readable memory;
recording whether all required memory resources are in a proper location in the coprocessor-readable memory, wherein said recording generates an indicator memory resource that is associated with the task;
processing... ...the beginning of processing the task, wherein if said indicator resource indicates that all required memory resources are not in a proper location in the coprocessor-readable memory , the coprocessor stops processing the task.
16. A method according to claim 15 wherein the... ...the coprocessor stopped processing, so that all required memory resources can be brought to a proper location in coprocessor-readable memory at a later time.
20. A method according to claim 19 wherein the later time...

7/3K/2 (Item 2 from file: 348) Links
   Fulltext available through: Order File History
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01778479
Multithreaded kernel for graphics processing unit
Mehrfadenkernel fur graphische Verarbeitungseinheit
Noyau multifiliere pour unite de traitement graphique

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	Country	Number	Kind	Date	
Patent	EP	1450257	A2	20040825	(Basic)
	EP	1450257	A2	20040825	
	EP	1450257	A3	20070905	
Application	EP	2004003537		20040217	
Priorities	US	448402	P	20030218	
	US	448399	P	20030218	
	US	448400	P	20030218	
	US	474513	P	20030529	
	US	763777		20040122	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LI; LU; MC;
NL; PT; RO; SE; SI; SK; TR;
Extended Designated States:
AL; LT; LV; MK;
International Patent Class (V7): G06F-009/48; G06F-009/50

IPC	Level	Value	Position	Status	Version	Action	Source	Office
G06F-0009/48	A	I	F	B	20060101	20040702	H	EP
G06F-0009/50	A	I	L	B	20060101	20040702	H	EP

Abstract Word Count: 137
NOTE: 2
NOTE: Figure number on first page: 2

Type	Pub. Date	Kind	Text
Publication: English			
Procedural: English			
Application: English			

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200435	2684

SPEC A	(English)	200435	20021
Total Word Count (Document A) 22710			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 22710			

Specification: ...Paging" refers to changing the physical address of a block of memory (a page) using mapping hardware. A paging buffer, generally speaking, is a DMA buffer that contains coprocessor instructions to... ...buffer to a correct memory location, from which those resources can be accessed by the coprocessor when needed. If a paging buffer is properly generated, the location of any requisite memory resources for a particular coprocessor task(i.e., a DMA buffer) is known.

Step 15 represents notification to a preparation thread that a paging buffer has... ...to conduct further preparation operations on a DMA buffer prior to sending it to a coprocessor for processing. For example, since memory locations may have changed since the creation of the original DMA buffer, the scheduler may... ...buffer with the actual location of memory resources. Finally, the scheduler may submit both the paging buffer (if it exists) and the DMA buffer to the coprocessor (and any other auxiliary hardware) to be processed.

Steps 1 through 16 as described above...

7/3K/3 (Item 1 from file: 349) Links
   Fulltext available through: Order File History
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01313061
METHOD FOR AT LEAST PARTIALLY COMPENSATING FOR ERRORS IN INK DOT PLACEMENT DUE TO ERRONEOUS ROTATIONAL DISPLACEMENT
PROCEDE POUR LA COMPENSATION AU MOINS PARTIELLE D'ERREURS DANS LE PLACEMENT POINTS D'ENCRE DUES A UN DEPLACEMENT ROTATIONNEL ERRONE

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	Country	Number	Kind	Date
Patent	WO	2005120835	A1	20051222
Application	WO	2004AU706		20040527
Priorities	WO	2004AU706		20040527

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG;
BR; BW; BY; BZ; CA; CH; CN; CO; CR; CU;
CZ; DE; DK; DM; DZ; EC; EE; EG; ES; FI;
GB; GD; GE; GH; GM; HR; HU; ID; IL; IN;
IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR;
LS; LT; LU; LV; MA; MD; MG; MK; MN; MW;
MX; MZ; NA; NI; NO; NZ; OM; PG; PH; PL;
PT; RO; RU; SC; SD; SE; SG; SK; SL; SY;
TJ; TM; TN; TR; TT; TZ; UA; UG; US; UZ;
VC; VN; YU; ZA; ZM; ZW;
[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PL; PT; RO; SE; SI; SK; TR;
[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;
[AP] BW; GH; GM; KE; LS; MW; MZ; NA; SD; SL;
SZ; TZ; UG; ZM; ZW;
[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 618378
Claims:
...the endpoint's buffer in DRAM. Conversely, all IN data packets are transferred from a buffer in DRAM to the local
packet buffers, and from there to the UDC20. The UDU's DMA controller handles all of this... ...describe streaming and
non-strearning modes respectively. Each IN or OUT endpoint's buffer in DRAM can be configured to operate as either a
circular buffer or a double buffer. Each IN and OUT endpoint has two DMA descriptors, A and B, which are used...

7/3K/4 (Item 2 from file: 349) Links
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01129704
DEAD NOZZLE COMPENSATION
COMPENSATION D'UNE BUSE HORS ETAT DE FONCTIONNEMENT

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	Country	Number	Kind	Date
Patent	WO	200450369	A1	20040617
Application	WO	2003AU1616		20031202
Priorities	AU	2002953134		20021202
	AU	2002953135		20021202

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PT; RO; SE; SI; SK; TR;
[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;
[AP] BW; GH; GM; KE; LS; MW; MZ; SD; SL; SZ;
TZ; UG; ZM; ZW;
[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 387411
Claims:
...by flushing the relevant cache lines, and so there is no hardware support to enforce cache coherency.
12 4 ISI transmit buffer arbitrationThe SCB control logic will arbitrate access to... ...ISI Tx packets:CPUISITxBuffer,
contained in the SCB control block. ISI mapped USB EP OUT buffers, contained in the USB device block. This arbitration
is controlled by the ISITxBuffArb register which...

?